AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) An apparatus comprising:

an antenna;

an amplifier unit connected to the antenna, wherein the amplifier unit includes a first amplifier and a second amplifier, wherein the first amplifier and the second amplifier each include a source, a drain, and a gate, respectively, wherein the gate of the first amplifier and the gate of the second amplifier are connected to a common gate connection, wherein the drain of the first amplifier and the drain of the second amplifier are connected to a common drain connection, and wherein the drain of the first amplifier is connected to the gate of the second ~~amplifier~~ amplifier;

a first switch that connects a transmit path of the antenna to the amplifier unit;

a second switch that connects a receive path of the antenna to the amplifier unit; and

a switch controller that is programmed to adjust positions of the first and second switches so that the amplifier unit is connected to the transmit or receive path of the antenna after a predetermined amount of time has elapsed since a prior adjustment.

2. (Previously Presented) The apparatus of claim 1, wherein the first switch has an output connected to the amplifier unit, a first input connected to the receive path and a second input connected to the transmit path.

3. (Previously Presented) The apparatus of claim 2, wherein the second switch has a first switch position connecting a signal for transmission to the antenna, and a second switch position connecting the receive path to the antenna.

4. (Previously Presented) The apparatus of claim 3, wherein the switch controller controls the first and second switches to selectively connect the antenna to the amplifier unit for amplification of a received signal and the amplifier unit to the antenna for amplification of a signal for transmission.

5. (Previously Presented) The apparatus of claim 1, wherein the amplifier unit comprises a third amplifier including a source, a drain, and a gate, wherein the gate of the third amplifier is connected to the common gate connection, wherein the drain of the third amplifier is connected to the common drain connection, and wherein the drain of the second amplifier is connected to the gate of the third amplifier.

6. (Previously Presented) The apparatus of claim 1, wherein the amplifiers are wide band gap high electron mobility transistors.

7. (Previously Presented) The apparatus of claim 1, wherein the amplifiers are monolithic microwave integrated circuits.

8. (Currently Amended) A method for transmission and reception of signals using a transceiver that includes an antenna, first and second switches, and an amplifier unit, wherein the amplifier unit includes a first amplifier and a second amplifier, wherein the first amplifier and the second amplifier each include a source, a drain, and a gate, respectively, wherein the gate of the first amplifier and the gate of the second amplifier are connected to a common gate connection, wherein the drain of the first amplifier and the drain of the second amplifier are connected to a common drain connection, and wherein the drain of the first amplifier is connected to the gate of the second amplifier, the method comprising:

setting the first switch to a first position of the first switch, the first position of the first switch connecting a first signal for transmission of the first signal to the amplifier unit for amplification of the first signal;

setting the second switch to a first position of the second switch, the first position of the second switch connecting the amplified first signal for transmission of the amplified first signal to the antenna;

~~setting the second switch, after a predetermined amount of time, to a second position, the second position connecting a signal received from the antenna to a receive path of the transceiver; and~~

setting the first switch, after [[the]] a predetermined amount of time, to a second position of the first switch, the second position of the first switch connecting

the receive path to the amplifier unit for amplification of a second signal received from the antenna; and

setting the second switch, after the predetermined amount of time, to a second position of the second switch, the second position of the second switch connecting the amplified second signal for further processing of the amplified second signal.

9. (Currently Amended) The method of claim 8, ~~wherein~~ wherein, when the second switch is in the second ~~position~~ position, the amplified second signal from the receive path is connected to receiver circuitry configured to perform the further processing.

10. (Cancelled)

11. (Previously Presented) The method of claim 8, wherein the amplifier unit is an AlGaN amplifier unit.

12-15. (Cancelled)

16. (Currently Amended) The apparatus of claim [[12,]] 18, wherein the amplifier is an AlGaN amplifier.

17. (Previously Presented) The apparatus of claim 1, wherein the amplifier is an AlGaN amplifier unit.

18. (New) An amplifier unit, comprising:

a first amplifier and a second amplifier, wherein the first amplifier and the second amplifier each include a source, a drain, and a gate, respectively,

wherein the gate of the first amplifier and the gate of the second amplifier are connected to a common gate connection,

wherein the drain of the first amplifier and the drain of the second amplifier are connected to a common drain connection, and

wherein the drain of the first amplifier is connected to the gate of the second amplifier.

19. (New) The amplifier unit of claim 18, wherein the drain of the first amplifier is connected to the gate of the second amplifier through a capacitor.

20. (New) The amplifier unit of claim 18, comprising:

a first bias current connected to the common drain connection;

a second bias current connected to the common gate connection; and

a ground connected to the source of the first amplifier and the source of the second amplifier.

21. (New) The amplifier unit of claim 18, comprising a third amplifier including a source, a drain, and a gate,

wherein the gate of the third amplifier is connected to the common gate connection,

wherein the drain of the third amplifier is connected to the common drain connection, and

wherein the drain of the second amplifier is connected to the gate of the third amplifier.

22. (New) An amplifier unit, comprising:

a first transistor and a second transistor,

wherein the first transistor and the second transistor each include a first terminal, a second terminal, and a third terminal, respectively,

wherein a respective voltage applied to the third terminal of each respective transistor controls current flow between the first terminal and the second terminal,

wherein the third terminal of the first transistor and the third terminal of the second transistor are connected to a first common terminal connection,

wherein the second terminal of the first transistor and the second terminal of the second transistor are connected to a second common terminal connection, and

wherein the second terminal of the first transistor is connected to the third terminal of the second transistor.

23. (New) The amplifier unit of claim 22, wherein the second terminal of the first transistor is connected to the third terminal of the second transistor through a capacitor.

24. (New) The amplifier unit of claim 22, comprising:

a first bias current connected to the first common terminal connection;

a second bias current connected to the second common terminal connection; and

a ground connected to the first terminal of the first transistor and the first terminal of the second transistor.

25. (New) The amplifier unit of claim 22, comprising a third transistor including a first terminal, a second terminal, and a third terminal,

wherein a voltage applied to the third terminal controls current flow between the first terminal and the second terminal,

wherein the third terminal of the third transistor is connected to the first common terminal connection,

wherein the second terminal of the third transistor is connected to the second common terminal connection, and

wherein the second terminal of the second transistor is connected to the third terminal of the third transistor.